**SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY**
**(AUTONOMOUS), PUTTUR**

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**QUESTION BANK (DESCRIPTIVE)**

**Subject with Code** : DIGITAL CIRCUITS (23EC0447)
**Course & Branch:** B. Tech –EEE
**Year & Semester:** III - B. Tech. & I-Semester **Regulation:** R23

## UNIT I
## LOGIC SIMPLIFICATION AND COMBINATIONAL LOGIC DESIGN

### PART-A (2 MARKS)

| | | | |
|---|---|---|---|
| **1.** | State De-Morgan's theorem. | **[L1][CO1]** | **[2M]** |
| **2.** | What is the concept of duality in Boolean algebra. | **[L1][CO1]** | **[2M]** |
| **3.** | Express the function Y=A+B'C in canonical POS. | **[L1][CO2]** | **[2M]** |
| **4.** | Simplify the following Boolean expression into one literal.<br>W'X (Z'+YZ) + X (W+Y'Z). | **[L2][CO2]** | **[2M]** |
| **5.** | Show how to connect NAND gates to get an AND gate and OR gate? | **[L2][CO1]** | **[2M]** |

### PART-B (10 MARKS)

| | | | | |
|---|---|---|---|---|
| 1. | (a) | State and prove the De-Morgan's Theorem with truth tables. | [L3][CO1] | [5M] |
| | (b) | State and prove the Consensus theorem. | [L3][CO1] | [5M] |
| 2. | | Simplify the following Boolean expression:<br>(a) F = (A+B)(A'+C)(B'+C').<br>(b) F = XY+XYZ+XYZ'+X'YZ | [L3][CO2] | [10M] |
| 3. | (a) | Simplify the following Boolean functions to minimum number of literals<br>(i) xyz + x'y + xyz'. (ii) xz + x'yz. | [L3][CO2] | [5M ] |
| | (b) | Simplify the following Boolean functions to minimum number of literals:<br>F = ABC + ABC' + A'B | [L3][CO2] | [5M ] |
| 4. | | Express the function Y=A+B'C in (i)Canonical SOP form (ii) Canonical POS form | [L2][CO1] | [10M] |
| 5. | | Explain about Logic gates. with symbols and truth tables. | [L2][CO1] | [10M] |
| 6 | | Minimize the following Boolean function using K-Map.<br>F(A, B, C, D)= Σm(0, 2, 4, 6, 8, 10, 12, 14). | [L3][CO1] | [10M] |
| 7. | | Simplify the following Boolean expressions using K-map.<br>F(A, B, C, D)= πM(0,2,3,8,9,12,13,15) | [L3][CO1] | [10M] |
| 8. | (a) | Simplify the following expression using the K-map for the 3-variable.<br>Y = AB'C+A'BC+A'B'C+A'B'C'+AB'C' | [L3][CO1] | [5M ] |
| | (b) | Simplify the following Boolean expressions using K-map.<br>F(A, B, C, D)= Σm(1,3,7,11,15) | [L3][CO1] | [5M ] |
| 9. | | Implement the function F(A,B,C,D) = Σ(0,2,5,7,8,10,13,15) using a 4-variable Karnaugh map | [L2][CO1] | [10M] |
| 10. | | Realize the Boolean function F(A,B,C) = Σ(0,1,2,5,7) using (i) AND-OR realization and (ii) NAND-only realization. | [L2][CO1] | [10M] |

## UNIT II
## INTRODUCTION TO COMBINATIONAL DESIGN 1

### PART-A (2 MARKS)

| | | | |
|---|---|---|---|
| **1.** | Determine the Boolean expression for a half adder and full adder | **[L1][CO2]** | **[2M]** |
| **2.** | State the principle of a BCD adder. | **[L1][CO2]** | **[2M]** |
| **3.** | Convert the binary number 1011 into Gray code | **[L1][CO3]** | **[2M]** |
| **4.** | Convert the Gray code 1101 into binary. | **[L1][CO3]** | **[2M]** |
| **5.** | What is the need for a seven-segment display decoder? | **[L1][CO3]** | **[2M]** |

### PART-B (10 MARKS)

| | | | | |
|---|---|---|---|---|
| **1.** | | Design & implement Half Adder and Full Adder with truth table. | **[L3][CO3]** | **[10M]** |
| **2.** | | Design & implement Half Subtractor and Full Subtractor with truth table**.** | **[L3][CO3]** | **[10M]** |
| **3.** | | Design a BCD adder using two 4-bit binary adders and necessary correction logic. | **[L3][CO3]** | **[10M]** |
| **4.** | | Design of a 4-bit binary-to-gray code converter with truth table and logic circuit. | **[L2][CO3]** | **[10M]** |
| **5.** | | Explain the concept of BCD addition and design a BCD adder circuit. | **[L2][CO3]** | **[10M]** |
| **6.** | | Distinguish between half adder and full adder with circuit diagrams. | **[L2][CO3]** | **[10M]** |
| **7.** | | Design of a 4-bit gray-to-binary code converter with truth table and logic circuit. | **[L2][CO3]** | **[10M]** |
| **8.** | | Write short notes on:<br>(a) Half adder and full adder<br>(b) Binary subtractor<br>(c) Seven-segment display | **[L2][CO3]** | **[10M]** |
| **9.** | | Design a BCD to Excess-3 code converter using logic gates. | **[L3][CO3]** | **[10M]** |
| **10.** | | Explain with truth table the working of a BCD to seven-segment display decoder and k- map for segments a, b and Draw the logic circuit. | **[L2][CO3]** | **[10M]** |

## UNIT III
## COMBINATIONAL LOGIC DESIGN 2

### PART-A (2 MARKS)

| | | | |
|---|---|---|---|
| **1.** | Define a decoder and mention one of its applications. | **[L1][CO4]** | **[2M]** |
| **2.** | What is a priority encoder? Give an example of its use. | **[L1][CO4]** | **[2M]** |
| **3.** | State the difference between multiplexer and demultiplexer. | **[L1][CO4]** | **[2M]** |
| **4.** | Write the truth table of a 2-bit comparator. | **[L1][CO4]** | **[2M]** |
| **5.** | Mention one real-life application of a demultiplexer. | **[L1][CO4]** | **[2M]** |

### PART-B (10 MARKS)

| | | | | |
|---|---|---|---|---|
| **1.** | | What is Decoder? Design the circuit for 3to 8 decoder with truth table. | **[L1][CO4]** | **[10M]** |
| **2.** | | What is Encoder? Design the circuit for Octal to Binary encoder with truth table. | **[L1][CO4]** | **[10M]** |
| **3** | | What is Priority Encoder? Design 4 input Priority Encoder. | **[L1][CO4]** | **[10M]** |
| **4.** | | Design 32:1 Mux using two 16:1 Muxs and one 2:1 Mux. | **[L3][CO4]** | **[10M]** |
| **5** | | What is Demultiplexer? Desingn1:8 Demultiplexer using 1:4 Demultiplexers. | **[L2][CO4]** | **[10M]** |
| **6.** | (a) | Write the difference between Multiplexer and De-multiplexer. | **[L2][CO4]** | **[5M ]** |
| | (b) | Design the 4:1 MUX and explain its operation in detail. | **[L3][CO4]** | **[5M ]** |
| **7.** | | Implement the following function F(A,B,C)=Σm(1,3,5,6) using (i) 16:1 MUX and (ii) 8:1 MUX | **[L2][CO4]** | **[10M]** |
| **8.** | | What is magnitude comparator? Design 2-bit comparator by using logic gates. | **[L1][CO4]** | **[10M]** |
| **9.** | | Design a logic circuit to implement the function $F(A, B, C, D) = \Sigma\, m(1, 3, 4, 11, 12, 13, 14, 15)$ using a 3-to-8 decoder and external gates. Show the steps. | **[L3][CO4]** | **[10M]** |
| **10.** | | Minimize the function $F(A, B, C, D) = \Sigma\, m(1, 3, 4, 11, 12, 13, 14, 15)$ and implement it using an 8-to-1 multiplexer. | **[L2][CO4]** | **[10M]** |

## UNIT IV
## SEQUENTIAL LOGIC DESIGN

### PART-A (2 MARKS)

| | | | |
|---|---|---|---|
| **1.** | Define a latch. | **[L1][CO5]** | **[2M]** |
| **2.** | Draw the truth table of an SR latch. | **[L1][CO5]** | **[2M]** |
| **3.** | What is a ripple counter? Why is it called asynchronous? | **[L1][CO5]** | **[2M]** |
| **4.** | Why is the master-slave configuration used in JK flip-flops? | **[L1][CO5]** | **[2M]** |
| **5.** | Define a shift register. List its types. | **[L1][CO5]** | **[2M]** |

### PART-B (10 MARKS)

| | | | | |
|---|---|---|---|---|
| 1. | | Draw and explain the circuit of an SR flip-flop using NAND gates. | **[L2][CO5]** | **[10M]** |
| 2. | | Design a D flip-flop. Explain its truth table and applications | **[L3][CO5]** | **[10M]** |
| 3. | | Implement a JK flip-flop using NAND gates and explain its operation. | **[L2][CO5]** | **[10M]** |
| 4. | | Explain the working of a T flip-flop with logic circuit and characteristic table. | **[L2][CO5]** | **[10M]** |
| 3. | | What is a Master-Slave JK flip-flop? Explain its operation with neat diagram. | **[L2][CO5]** | **[10M]** |
| 4. | | Distinguish between level triggered and edge triggered flip-flops with diagrams. | **[L2] [CO5]** | **[10M]** |
| 5. | | Explain how a T flip-flop can be realized using a JK flip-flop. | **[L2][CO5]** | **[10M]** |
| 6. | | Design a 4-bit asynchronous ripple counter using T flip-flops. | **[L3][CO5]** | **[10M]** |
| 7. | | What are universal shift registers? Explain with a block diagram. | **[L1][CO5]** | **[10M]** |
| 8. | | Define setup time and hold time of a flip-flop. With the help of a timing diagram, explain the consequences of violating these requirements. | **[L2][CO5]** | **[10M]** |
| 9. | | Design and implement 3-bit ripple counter using J-K flip flop. Draw the state diagram, logic diagram and timing diagram for the same. | **[L3][CO5]** | **[10M]** |
| 10. | | Design a serial-in parallel-out (SIPO) shift register with logic diagram. | **[L2][CO5]** | **[10M]** |

## UNIT V
## PROGRAMMABLE LOGIC DEVICES AND DIGITAL IC'S

### PART-A (2 MARKS)

| | | | |
|---|---|---|---|
| **1.** | Write the difference between PROM and PLA. | **[L1][CO6]** | **[2M]** |
| **2.** | Mention two applications of ROM. | **[L1][CO6]** | **[2M]** |
| **3.** | What is the function of the IC 74x138? | **[L1][CO6]** | **[2M]** |
| **4.** | State the number of data select inputs in a 74x155 demultiplexer. | **[L1][CO6]** | **[2M]** |
| **5.** | State one difference between a decoder and a demultiplexer. | **[L1][CO6]** | **[2M]** |

### PART-B (10 MARKS)

| | | | | |
|---|---|---|---|---|
| 1. | | What is ROM organization? Explain about Different types of ROM. | **[L1][CO6]** | **[10M]** |
| 2. | | Explain the working of a PLA (Programmable Logic Array) with example. | **[L2][CO6]** | **[10M]** |
| 3. | | Compare three combinational circuits: PLA, PAL and PROM | **[L3][CO6]** | **[10M]** |
| 4. | | Implement PLA circuit for the following functions F1(A,B,C)= Σm(3,5,6,7), F2(A,B,C)= Σm(0,2,4,7). | **[L2][CO6]** | **[10M]** |
| 5. | | Implement the following Boolean function using PAL.<br>(i)W(A,B,C,D) = Σm(0,2,6,7,8,9,12,13) (ii)X(A,B,C,D) = Σm(0,2,6,7,8,9,12,13,14) | **[L2][CO6]** | **[10M]** |
| 6. | | Implement the Boolean function F(A,B,C)=Σ(1,3,5,7) using IC 74x138 decoder. | **[L2][CO6]** | **[10M]** |
| 7. | | Implement the function F(A,B,C,D)=Σ(0,2,4,6,8,10,12,14) using 74x151 multiplexer. | **[L2][CO6]** | **[10M]** |
| 8. | | Describe the function of IC 74x148 Priority Encoder with logic diagram. | **[L3][CO6]** | **[10M]** |
| 9. | | Explain the working principle of a 1-to-4 demultiplexer with IC 74x155 as example. | **[L2][CO6]** | **[5M]** |
| 10. | | Draw and explain the internal structure of Comparator IC 74x85. | **[L3][CO6]** | **[5M]** |

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